CLAIMS (with indication of amended or new):

4. (Amended) A PLL frequency synthesizer according to claim 12, further comprising a buffer amplifier for protecting the voltage-controlled oscillator from an abrupt variation at a load portion of the PLL frequency synthesizer.

11. (New) A PLL frequency synthesizer which outputs a signal having a desired frequency, comprising:

a voltage-controlled oscillator (VCO) for generating an output signal having a voltage and a frequency;

a phase comparator for comparing a phase of the frequency of the VCO generated output signal with a phase of a frequency of a reference signal and outputting a difference signal; and

a charge pump for producing an output signal in response to the difference signal output from the phase comparator and for driving the VCO, wherein the voltage of the output signal from the charge pump is within predetermined driving limits, and

wherein when the charge pump output signal voltage changes to a value close to one of the driving limits thereof, both the output signal from the charge pump and a power supply signal having a voltage which cancels the change are inputted to the VCO, thereby maintaining stability of the output signal from the VCO.

12. (New) A PLL frequency synthesizer which outputs a signal having a set frequency, comprising:

a voltage-controlled oscillator (VCO) for generating an output signal having a voltage and a frequency;

a phase comparator for comparing a phase of the frequency of the VCO generated output signal with a phase of a frequency of a reference signal and outputting a difference signal; and

a charge pump for producing an output signal in response to the difference signal output from the phase comparator,

wherein the VCO is driven by the output signal from the charge pump and a power supply signal having a voltage controlled based on the set frequency, to thereby widen an apparent lock range of the PLL.

13. (New) A radio communication apparatus comprising a PLL frequency synthesizer which outputs a signal having a desired frequency, the PLL frequency synthesizer including:

a voltage-controlled oscillator (VCO) for generating an output signal having a voltage and a frequency;

a phase comparator for comparing a phase of the frequency of the VCO generated output signal with a phase of a frequency of a reference signal and outputting a difference signal; and

a charge pump for producing an output signal in response to the difference signal output from the phase comparator and for driving the VCO, wherein the voltage of the output signal from the charge pump is bound within predetermined driving limits, and

wherein when the charge pump output signal voltage changes to a value close to one of the driving limits thereof, both the output signal from the charge pump and a power supply signal having a voltage which cancels the change are inputted to the VCO, thereby maintaining stability of the output signal from the VCO.

14. (New) A radio communication apparatus comprising a PLL frequency synthesizer which outputs a signal having a set frequency, the PLL frequency synthesizer including:

a voltage-controlled oscillator (VCO) for generating an output signal having a voltage and a frequency;

a phase comparator for comparing a phase of the frequency of the VCO generated output signal with a phase of a frequency of a reference signal and outputting a difference signal; and

a charge pump for producing an output signal in response to the difference signal output from the phase comparator,

wherein the VCO is driven by the output signal from the charge pump and a power supply signal having a voltage controlled based on the set frequency, to thereby widen an apparent lock range of the PLL.

15. (New) The radio communication apparatus of claim 14, wherein the PLL frequency synthesizer further includes a buffer amplifier for protecting the voltage-controlled oscillator from the an abrupt variation at a load portion of the PLL frequency synthesizer.